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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte MICHAEL O. THOMPSON, RICHARD WOMACK,
JOHAN CARLSSON, and GORAN GUSTAFSSON

Appeal 2009-014368
Application 10/088,913
Technology Center 2800

Before KRISTEN L. DROESCH, JASON V. MORGAN, and
ERIC B. CHEN, *Administrative Patent Judges*.

MORGAN, *Administrative Patent Judge.*

DECISION ON APPEAL

STATEMENT OF THE CASE

Introduction

This is an appeal under 35 U.S.C. § 134(a) from the Examiner's final rejection of claims 1 – 5 and 12 – 16. We have jurisdiction under 35 U.S.C. § 6(b). We affirm.

Exemplary Claim

> 1. A non-volatile passive matrix memory device comprising;
>
> an electrically polarizable dielectric memory material exhibiting hysteresis, wherein said memory material is provided sandwiched in a layer between a first set and second set of respective parallel addressing electrodes, wherein the electrodes of the first set constitute word lines of the memory device and are provided in substantially orthogonal relationship to the electrodes of the second set, the latter constituting bit lines of the memory device,
>
> wherein a memory cell with a capacitor-like structure is defined in the memory material at the crossings between word lines and bit lines, wherein the memory cells of the memory device constitute the elements of a passive matrix, wherein each memory cell can be selectively addressed for a write/read operation via a word line and bit line, where each memory cell is at all times in physical contact with a word line and a bit line,
>
> wherein a write operation to a memory cell takes place by establishing a desired polarization state in the cell by means of a voltage being applied to the cell via the respective word line and bit line defining the cell, wherein said applied voltage either establishes a determined polarization state in the memory cell or is able to switch between the polarization states thereof, and wherein a read operation takes place by applying a voltage larger than the coercive voltage Vc, to the memory cell and

> detecting at least one electrical parameter of an output current on the bit lines,
>
> wherein the word lines are divided into a number of segments, each segment including and being defined by a plurality of adjoining bit lines in the matrix, each word line in a segment is differentiated based on the position of the word line within the segment, each word line in the segment being adjoined to a separate bit line, where each separate bit line assigned to a segment is connected with a different associated sensing means, such that a word line of the same position within each segment is selected within each segment, each word line of the same position being sensed at the same time by said respective different associated sensing means, thus enabling simultaneous connection of all memory cells assigned to a word line on a segment for readout via the corresponding bit lines of the segment, each sensing means being adapted for sensing the charge flow in the bit line connected therewith in order to determine a logical value stored in the memory cell defined by the bit line.

ISSUE

Are the 35 U.S.C. § 103(a) rejections of claims 1, 13, 14, 16, and 17 unsustainable because the Examiner erred in finding that the combination of Kuroda (U.S. 5,487,029) and Clemons (U.S. 4,599,709) teaches or suggests memory cells of a memory device that are at all times in physical contact with a word line and a bit line?

Are the 35 U.S.C. § 103(a) rejections of claims 1, 13, 14, 16, and 17 unsustainable because the Examiner erred in concluding that it would have been obvious to an artisan of ordinary skill to combine the teachings and suggestions of Kuroda and Clemons?

ANALYSIS

We have reviewed the Examiner's rejections in light of Appellants' arguments (Appeal Brief) that the Examiner has erred.

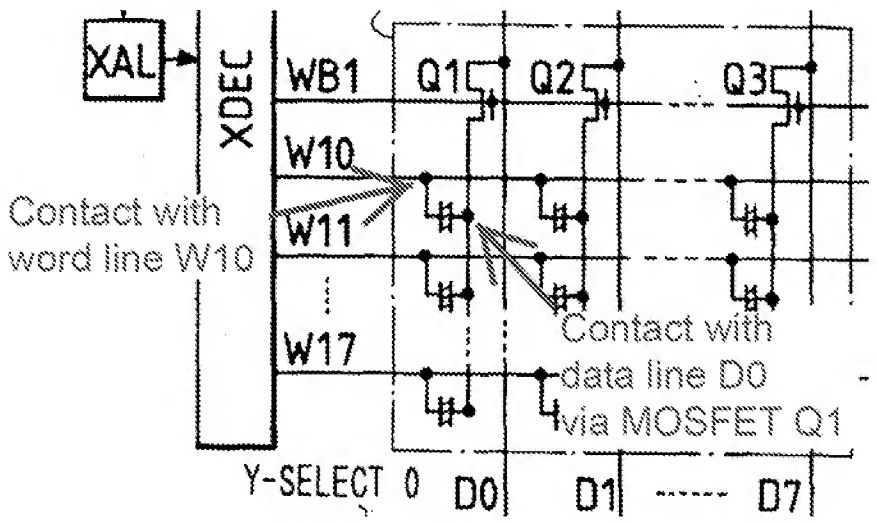
We disagree with Appellants' conclusions. We adopt as our own the findings and reasons set forth by the Examiner in the action from which this appeal is taken and in the Examiner's Answer in response to Appellants' Appeal Brief. We concur with the conclusions reached by the Examiner.

Whether the Examiner erred in finding that the combination of Kuroda and Clemons teaches or suggests memory cells of a memory device that are at all times in physical contact with a word line and a bit line

Claims 1 and 12 recite memory cells that are "at all times in *physical contact* with a word line and a bit line" (emphasis added). Similarly, claim 13 recites memory material that "is at all times in *physical contact* with the first and second set of electrodes" (emphasis added).

Appellants submit that "a passive matrix memory requires the ferroelectric material of the capacitor be at all the time . . . in ohmic contact with the metal electrodes" (App. Br. 15). However, as the Examiner points out (Ans. 3), "ohmic contact" is not found in the claim recitations. Instead, the claims merely require "physical contact." The broadest reasonable interpretation of "physical contact" encompasses any physical connection between the memory cells and the claimed lines.

The requisite physical connections are depicted in Kuroda's figure 1, an excerpt of which is depicted below:



The excerpt of Kuroda's figure 1, depicted above, shows part of a semiconductor memory system (col. 3, ll. 18 – 20). Annotations have been added to show where a memory cell, depicted as a ferroelectric capacitor, makes a physical connection with word line W10 and, through MOSFET Q1, with data line D0. Kuroda discloses a physical connection between the memory cell and the word line W10. MOSFET Q1 does not always allow for *electrical* contact between the memory cell and the data line D0 (i.e., when MOSFET Q1 is switched off). However, MOSFET Q1 does maintain continuous *physical* contact between the memory cell and the data line.

Accordingly, we agree with the Examiner (Ans. 4 and 11 – 13) that Kuroda teaches or suggests memory cells (ferroelectric capacitors) that are at all times in physical contact with a word line (W10 – W17) and a bit line (D0 – D7) (fig.1).

Whether the Examiner erred in concluding that it would have been obvious to an artisan of ordinary skill to combine the teachings and suggestions of Kuroda and Clemons

Appellants argue that it would not have been obvious to combine the teachings and suggestions of Kuroda and Clemons because "Kuroda does

not allow for parallel readout. Only a single memory cell of a single circuit in one block of a column of blocks is read at a time" (App. Br. 18). However, Kuroda discloses that the disclosed memory system "is adapted to write/read data at the unit of 8 bits" (col. 6, ll. 4 – 5).

This parallel read out of eight bits at a time is possible because Kuroda discloses a "memory array portion provided with eight memory blocks in the row direction and with two memory blocks in the column direction" (col. 6, ll. 7 – 9). Only four of the sixteen memory blocks are depicted, with BLOCK (1, 0) the only block where the memory cells themselves are detailed (fig.1; col. 6, ll. 11 – 12). "The eight memory blocks arranged in the row direction are made to correspond to eight data terminals DIO-**0** to DIO-**7**" (col. 6, ll. 9 – 11).

Because Kuroda depicts the readout of the contents of eight memory cells at a time, not just of a single memory cell, we agree with the Examiner that Kuroda discloses parallel readout of memory cells (Ans. 12 – 13 and 15 – 16).

We also agree with the Examiner that it would have been obvious to an artisan of ordinary skill at the time of the invention to combine the teachings and suggestions of Kuroda and Clemons (Ans. 5 – 6 and 15 – 20). At the time of the invention, adapting a non-volatile passive matrix memory device comprising ferroelectric memory cells (as taught by Kuroda) with an improved multiplexing arrangement (as taught by Clemons) would have been obvious to one with ordinary skill in the art since the combination of familiar elements according to known methods is obvious when it does no more than yield a predictable result. *See KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398, 416 (2007).

Accordingly, we sustain the rejection of independent claims 1 and 13 under 35 U.S.C. § 103(a). Claims 14, 16, and 17 depend from independent claims 1 and 13 and Appellants have not presented any substantive arguments with respect to these claims. Therefore, we sustain the rejection of claims 14, 16, and 17 under 35 U.S.C. § 103(a) for the same reasons discussed with respect to independent claims 1 and 13.

Appellants do not argue with specificity for separate patentability of claims 2 – 5, 12, 15, and 18. Accordingly, we also sustain the rejections of these claims.

CONCLUSIONS

The Examiner has demonstrated that claims 1 – 5 and 12 – 16 are unpatentable because the Examiner did not err in finding and concluding:

that the combination of Kuroda and Clemons teaches or suggests memory cells of a memory device that are at all times in physical contact with a word line and a bit line and

that it would have been obvious to an artisan of ordinary skill to combine the teachings and suggestions of Kuroda and Clemons.

DECISION

We affirm the Examiner's decision rejecting claims 1 – 5 and 12 – 16.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

msc